WHAT IS CLAIMED IS:

1. An apparatus including a programmable logic device, said programmable logic device comprising:

a memory that stores configuration information and user defined information, wherein said memory selectively operates according to a first power state and a second power state, wherein said second power state is a lower power consumption state than said first power state; and

a control circuit, coupled to said memory, that controls access to said memory with a power selection signal, wherein said first power state corresponds to accessing said memory at a first rate and said second power state corresponds to accessing said memory at a second rate,

wherein during configuration of said programmable logic device, said control circuit controls said memory to output said configuration information at said first rate, and

wherein during normal operation of said programmable logic device, said control circuit controls said memory to selectively access said user defined information at one of said first rate and said second rate in accordance with said power selection signal, wherein said second rate is lower than said first rate.

2. The apparatus of claim 1, wherein said memory comprises a flash nonvolatile memory.

3. The apparatus of claim 1, wherein said memory comprises an electrically erasable programmable read only memory (EEPROM).

4. The apparatus of claim 1, wherein said control circuit comprises:

a first sense amplifier, coupled to said memory, that reads first information from said memory at said first rate, wherein said first sense amplifier is responsive to said power selection signal and operates according to said first power state;

a second sense amplifier, coupled to said memory, that reads second information from said memory at said second rate, wherein said second sense amplifier is responsive to said power selection signal and operates according to said second power state; and

a data selector, coupled to said first sense amplifier and said second sense amplifier, that selectively outputs an output of one of said first sense amplifier and said second sense amplifier, in accordance with said power selection signal.

5. The apparatus of claim 4, wherein said first sense amplifier comprises a high-power sense amplifier.

6. The apparatus of claim 4, wherein said second sense amplifier comprises a low-power sense amplifier.

7. The apparatus of claim 4, wherein said data selector comprises a multiplexer.

8. The apparatus of claim 1, wherein said programmable logic device further comprises:

a plurality of function blocks that perform a plurality of functions, wherein said plurality of function blocks includes said memory and said control circuit; and

an interconnect that interconnects said plurality of function blocks.

9. An apparatus including a control circuit for controlling a programmable logic device that includes a memory, said control circuit comprising:

a first sense amplifier, coupled to said memory, that reads first information from said memory at a first rate, wherein said first sense amplifier is responsive to a power selection signal and operates according to a first power state;

a second sense amplifier, coupled to said memory, that reads second information from said memory at a second rate, wherein said second sense amplifier is responsive to said power selection signal and operates according to a second power state; and

a data selector, coupled to said first sense amplifier and said second sense amplifier, that selectively outputs an output of one of said first sense amplifier and said second sense amplifier, in accordance with said power selection signal,

wherein said control circuit controls access to said memory with said power selection signal, wherein said first power state corresponds to accessing said memory at said first rate and said second power state corresponds to accessing said memory at said second rate,

wherein during configuration of said programmable logic device, said control circuit controls said memory to output configuration information at said first rate, and

wherein during normal operation of said programmable logic device, said control circuit controls said memory to selectively access user defined information at one of said first rate and said second rate in accordance with said power selection signal, wherein said second rate is lower than said first rate.

10. An apparatus including a programmable logic device, said programmable logic device comprising:

a plurality of function blocks that perform a plurality of functions, wherein said plurality of function blocks includes:

a memory that stores configuration information and user defined information, wherein said memory selectively operates according to a first power state and a second power state, and wherein said second power state is a lower power consumption state than said first power state, and

a control circuit that controls access to said memory with a power selection signal, wherein said first power state corresponds to accessing said memory at a first rate and said second power state corresponds to accessing said memory at a second rate; and

an interconnect that interconnects said plurality of function blocks,

wherein during configuration of said programmable logic device, said control circuit controls said memory to output said configuration information at said first rate, and

wherein during normal operation of said programmable logic device, said control circuit controls said memory to selectively access said user defined information at one of said first rate and said second rate in accordance with said power selection signal, wherein said second rate is lower than said first rate.

11. A method of operating a programmable logic device, comprising the steps of:

during configuration of said programmable logic device, selecting a first power state and outputting configuration information from a memory at a first rate;

after configuration during normal operation of said programmable logic device, selecting a second power state for selectively accessing said memory at a second rate, wherein

said second rate is lower than said first rate, and wherein said second power state is a lower power consumption state than said first power state; and

after configuration during normal operation of said programmable logic device, selecting said first power state for selectively accessing said memory at said first rate.